NEW HORIZON COLLEGE OF ENGINEERING, BANGALORE

(Autonomous College affiliated to VTU, Accredited by NAAC with Grade 'A' & NBA)

Department of Electronics and Communication Engineering

REPORTONGUESTLECTURE

Topic: BASICS OF VLSI LAYOUT DESIGN

A seminar on CMOS VLSI was conducted on the **24th of August 2019** by Ms Tabassum V Mulla, Senior Member of Technical Staff at Invecas Technologies, Bangalore with over 12 years of experience in the field of VLSI and Standard cell library development with expertise in standard cell library development in FinFETs. Ma'am is supervising the backend package of standard cell projects at Invecas Technologies. Ms Tabassum has also worked for other tech giants like ARM Embedded Technologies, Masamb Electronics and karmic, working for designated clients like Texas Instruments and Qualcomm. Over 50 students from the 5th semester attended this session.

The session was an interconnect between the industry and Academia. Ms Tabassum explained the difficulties that the present industry facing in **leakage currents and slews** in MOSFETS. Along with MOSFET a brief introduction to FinFETs was also given to us. To keep up with Moore's law, the size of the transistor had to be reduced. But at 28 nm, mainstream MOSFETs couldn't be used. So, FinFETs came into existence. FinFETs are 3 dimensional MOSFETs which the gate on 3 sides. This helped reduced the size even further down to the current 11 nm technology. Though the industry has kept us with Moore's Law, there are still problems associated with it like leakage current and static power loss.

Ms Tabassum explained to us why there is a bulk terminal on the MOSs. This is to control the channel along with the gate and to prevent latch-up which is an internal short-circuiting. Ms Tabassum also explained to us why today the layout designers play a key role in the success of a product in the market unlike how it was otherwise a few years ago. This is because a good layout would mean a lower delay compared to poorer layout design. This delay could be a few Pico seconds but, in the market, it makes a huge difference.

Overall, the session was interactive with activities like drawing outputs and estimating values of various parameters. Also, students were given some homework to research further on topics like FDSOI, Latch-up and technology which battery technologies use. Apart from the technicality, the students received tips on how to get into a core company and how to take advance their current knowledge on the subject. This session was organized by Dr Sanjeev Sharma, HoD, Department of Electronics and Communication and Ms. Dharmambal and Ms. Divya Sharma, Department of Electronics and Communication along with the support of Mr.G. Rajesh sir. A hearty thanks to them on behalf of all the students.