NEW HORIZON COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Miniproject II

Academic Year: 2017-18 **Semester: IV**

Sl. No	Semester	Project Batch Number	Name of the Student	Title of the project
1	IV	AG1	KIRAN N	GESTURE RECOGINISION TO CREATE VIRTUAL MOUSE
2	IV		KISHORE N	
3	IV	AG2	ATHIRA AJAY	AUTOMATIC SWITCH CONTROL USING MAT LAB
4	IV		LEHARIKA C	
5	IV		KUSHI PONNAMMA	
6	IV	AG3	AKSHAY RAO	ALARM CLOCK USING VERI LOG
7	IV		ANOOP A	
8	IV		ARUN P	
9	IV	AG4	G AVINASH	DESIGN OF RAM & ROM USING LOGIC CIRCUIT
10	IV		MADAN GOWDA M	
11	IV		MITHUN V	
12	IV	AG5	MANJUNATH N	CONVERTING MAT LAB CODE TO HDL USING SIMULINK
13	IV		MOHIT R	
14	IV		MEGA SHREE	
15	IV	AG6	KALAMADI SREE LEKHA	FPGA BASED PULSE DETECTION USING HIGH SPEED FFT
16	IV		K V MOUNISH REDDY	
17	IV		ARUNA C	
18	IV	AG7	AKHILESH VARMA	LINEAR MORPHOLOGY IMAGE PROCESSING USING HDL
19	IV		ANIL BHARATH	
20	IV		A SAI VENKAT THRIMOORTHY	
21	IV	AG8	ABHISHEK KUMAR	ULTRASONIC MAP MAKER USING MAT LAB & ARDUNIO
22	IV		KARTHIK KS	
23	IV		MANJUNATHA S	
24	IV	AG9	DEEPTHI R	GLUCOMA DETECTION BY MAT LAB
25	IV		MADHU M D	
26	IV		MISBAH T A	
27	IV	AG10	AFZAL HUSSAIN	CONTROL ARDUNIO USING MAT LAB
28	IV		DENNIS VINCENT PAUL RAJ	
29	IV		ASHISH KUMAR	
30	IV	AG11	CHETHAN S	NOISE SUPRESSION USING DSP PROCESSOR
31	IV		KIRAN C A	
32	IV		KIRAN R	
33	IV	AG12	ARATHI V	HOME AUTOMATION
34	IV		BAVANI V	
35	IV		SUPRITHA H C	

36	IV	AG13	A M AMARJITH	IMPLEMENTATION OF PREVENTING SYSTEM USING FPGA
37	IV		GIRIVARDHAN K	
38	IV		MOURYA REDDY Y	
39	IV	AG14	MOHITH SAHU	BLUE TOOTH BASED WIRELESS HOME AUTOMATION USING FPGA
40	IV		BIPIN DIXIT	
41	IV		HRASH SRIVASTAVA	
42	IV	AG15	LALITHAMBA	VGA BASED BOUNCING BALL INTERFACE USING FPGA
43	IV		JAHNAVI	
44	IV		MEGHNA V	
45	IV	AG16	HEMANTH KRISHNA	CAR PARKING SYSTEM USING VERILOG
46	IV		ANMOL	
47	IV		ALVIRA	
48	IV	AG17	MOHAMMED FAROOQ PASHA	ELECTRONIC VOTING MACHINE USING MAT LAB
49	IV		MOHAMMED ANAS	
50	IV		ELDO JOSE	
51	IV	AG18	BASKAR CHOUDHARY	GENERATION OF PPM AND PAM USING MATLAB
52	IV		ADITYA C	
53	IV		DEEPAK KUMAR	
54	IV	AG19	GIRISH GOWDA	AUDIO EQULIZER USING MATLAB
55	IV		HARI PRASAD R	
56	IV		JAGADISH D	
57	IV	AG20	JANANI B R	8 BIT ALU USING FPGA
58	IV		MANJULA	
59	IV		MEGHA SHREE	
60	IV	AG21	YUGANDAR REDDY	UART USING VERILOG
61	IV		SREEKANTH REDDY	
62	IV		RAJESH T A	
63	IV	AG22	DARSHAN RAJ	VHDL CODE FOR SINGLE PORT RAM
64	IV		MAHESHWARI N	
65	IV		KASIM	
66	IV	AG23	MUJEER PASHA	TEXT EXTRACT FROM IMAGE
67	IV		ASCHIT M	
68	IV	AG24	AKHIL JOSEPH	WIRELESS TEMPERATURE MONITORING SYSTEM
69	IV		ANUSH H N	
70	IV		DEPRAT	
71	IV	AG25	VICTOR ABHILASH	AUDIO EQULIZER
72	IV		CHADRAKIRAN REDDY	
73	IV		AKASH PRASAD	
74	IV	BG1	PRNAY REDDY D	TOUCH SCREEN CLOCK
75	IV		SIVACHELLA	
76	IV		VIJAYAKUMAR C	
77	IV	BG2	POOJA S NAIK	TIC TAK TOE GAME USING FPGA
78	IV		NISHU DUBEY	
79	IV		SINDHU C R	

80	IV	BG3	P MAHALAKSHMI	BILENEAR INTERPOLUTRY USING MATLAB
81	IV		SAI DEEPTHI T	
82	IV		SHAIK NOORULLA BASHA	
83	IV	BG4	S PAVANI	PROPELLER USING MATLAB
84	IV		VEENA K	
85	IV		PREM KUMAR	
86	IV	BG5	PRESHIKA J M	PCM USING MATLAB
87	IV		PRITHIPA A	
88	IV		RAKSHITHA N	
89	IV	BG6	NITESH K	PING PONG GAME USING VHDL
90	IV		ASHOK CHOUDHARY	
91	IV		BHARATH MVK	
92	IV	BG7	MAGDOOM FUAAD	KEYBOARD LEARNER USING SIMULINK 3 FPGA KIT
93	IV		SRIDHAR P	
94	IV	BG8	SPOORTHY G	DESIGN OF A NOTCH FILTER USING MATLAB
95	IV		YATHIN S	
96	IV		YESHWANTH M	
97	IV	BG9	SUSMA CHIKKUR	DESIGN OF ELEVATOR CONTROL USING VERILOG
98	IV		VIDHYA VISHNU	
99	IV		NAMRUTHA PRAKASH	
100	IV	BG10	JYOTHI CHANDRASHEKAR	TDM USING FPGA
101	IV		MONIKA T M	
102	IV		SUSHMITHA	
103	IV	BG11	NEHA MAHESH	IMAGE COMPRESSION USING MAT LAB
104	IV		DEEPAK P S	
105	IV		JAGAN MOHAN REDDY	
106	IV	BG12	PRAVEEN KUMAR S	VEDIC MULTIPLIER FOR 8 BIT NUMBER
107	IV		YESHWANTH J M	
108	IV		PRASHANTH GOWDA R S	
109	IV	BG13	NITHIN E	REAL TIME IMAGE PROCESSING ON FPGA USING VERILOG
110	IV		RISHAB S G	
111	IV		SHASHANK S	
112	IV	BG14	PARITHOSH V	SPEED DETECTION USING WEIGHT SENSOR
113	IV		ROSHINI M	
114	IV		VEDA M KULKARNI	
115	IV	BG15	SAAJU S P	RSA ALGORITHAM
116	IV		SREEPAD	
117	IV		SAI PRASHANTH	
118	IV	BG16	SHAMBULINGA PATIL	DIGITAL IC TESTER (MAT LAB)
119	IV		AKSHAY S	
120	IV	BG17	PAVAN KUMAR	DESIGN OF BASIC GATES USING QCA
121	IV		PAVAN RAJ	
122	IV		PRAJWAL T J	

123	IV	BG18	HABHISHEK T E	TESTING OF DIGITAL ICS USING FPGA
124	IV		SHAIK ASIF	
125	IV		SAI KIRAN	
126	IV	BG19	SRAVINI R S	OBJECT RECOGNITION USING MAT LAB
127	IV		SAM LENDER P	
128	IV		VIJAY C	
129	IV	BG20	SIDDESH L J	3 BIT ALU USING VHDL
130	IV		VIJAY S	
131	IV		VISHWANATH	
132	IV	BG21	SACHIN M	ANTENNA DESIGN FOR 5G
133	IV		SAGAR	
134	IV	BG22	RAJVARDHAN	FACE DETECTION USING MAT LAB
135	IV		VARUN MISHRA	
136	IV	BG23	SIMON CHOUHAN	SIMPLE CALUCULATOR USING FPGA
137	IV		UDIT BAHUGUNA	
138	IV		THANUJ A	
139	IV	BG24	SIDDARAMAPPA	TURN OFF STREET LIGHT USING MICRO CONTROLLER
140	IV		GURURAJ	
141	IV	BG25	YASHWANTH M L	JPG COMPRESSOR USING MAT LAB
142	IV		YATHISH	
143	IV	CG1	LINGRAJ J	HOME AUTOMATION USING FPGA
144	IV		NAVAS KHAN	
145	IV		PAVAN KUMAR S	
146	IV	CG2	AKSHAY V	COMBINATIONAL LOCK USING FPGA
147	IV		SHYAM S	
148	IV		SHASHANK RAO	
149	IV	CG3	MONICA E	HEXA POD SIMULATION USING MAT LAB
150	IV		NIVEDITHA N	
151	IV		SHRIYA G	
152	IV	CG4	ASHUTHOSH MANISH	DROSY DRIVER DETECTION USING MAT LAB
153	IV		GAGANA M R	
154	IV		TARUN SAI REDDY	
155	IV	CG5	ABUBAKER SIDDIQ	PAR BASED SECURITY ALERT SYSTEM(FPGA)
156	IV		JEEVAN K	
157	IV		REDDY SHEKAR B S	
158	IV	CG6	HARSHITHA P	MAKING RADAR USING ARDUNIO AND MAT LAB
159	IV		PRIYA DARSHINI M	
160	IV		POOJA P CHAUHAN	
161	IV	CG7	MITHUN KUMAR	VISITOR IN AND OUT COUNTER USING FPGA AND PIR SENSOR
162	IV		VAMSHI KRISHNA B	
163	IV		BALAJI L	

164	IV	CG8	CHIRAG S	PLL USING FPGA
165	IV		PRAVEEN KUMAR	
166	IV		LIKITH B M	
167	IV	CG9	YESHASWINI K N	AGE CALCULATION PROCESSING USING MAT LAB
168	IV		SWATHI K	
169	IV	CG10	VASANTH R	AUTOMATIC STREET LIGHT CONTROLLER
170	IV		JAYANTH V	
171	IV		JANARDHANA T	
172	IV	CG11	NISHA ANANDU NAIK	DESIGN OF FIR FILTER USING FPGA
173	IV		SINDHU A	
174	IV	CG12	GOWRI SNEHA PRIYA	SIGNATURE MONITORING USING MAT LAB
175	IV		SMITHA B S	
176	IV		RAMYA R	
177	IV	CG13	K RAGHAVENDRA	DATA ENCRIPTION USING MAT LAB
178	IV		PRAVEEN S	
179	IV	CG14	REGHU R	DESIGN AND ANALYSIS OF DIFFERENT ADDRESS USING FPGA
180	IV		RAKESH KUMAR T	
181	IV		NAVEEN KUMAR J	
182	IV	CG15	NIVEDITHA R	CRYPTOGRAHY CO PROCESSOR DESIGN IN VHDL
183	IV		PAVITHRA N	
184	IV		T R BOOMIKA	
185	IV	CG16	B N CHITHRA SREE	COLOUR &TEXTURE BASED IMAGE RETRIVAL
186	IV		B J KOUSALYA	
187	IV		MANASA C	
188	IV	CG17	PRATHAMESH K	DESIGN OF TRAFFIC LIGHT CONTROLLER USING FPGA
189	IV		RAHUL JAIN	
190	IV		CHIRANJEEVI	
191	IV	CG18	ANITA CHOUHAN	VENDING MACHINE
192	IV		ANJU GOPINATH	
193	IV	CG19	M ANISHA	CARRY SKIP ADDER USING FPGA
194	IV		RACHANA	
195	IV		RUCHIKA	
196	IV	CG20	MANJUNATH T	DISTANCE MEASUREMENT USING ULTRASONIC SENSOR(VHDL)
197	IV		MD. ZEESHAN ALI	
198	IV		S SARAVANA	
199	IV	CG21	ABHISHEK P	ULTRA SONIC DISH ANTENNA OBSTACLE DETECTION USING FPGA
200	IV		RITHVIK	
201	IV	CG22	ABHISHEK KHOT	AUDIO VISUALIZER BY FPGA
202	IV		TILAK PRASAD	
203	IV		MANOJ R	
204	IV	CG23	G V NIKESH	PIANO USING GUI IN MAT LAB
205	IV		M SIVA NAGA MUNI REDDY	
206	IV		YUVA SREE	

207	IV	CG24	VISHNU VIKAS	CPU FAN SPEED CONTROL BASED ON IC TEMPERATURE USING FPGA
208	IV		MAMATA V K	
210	IV	CG25	CHETHAN BR	TDM USING MAT LAB
211	IV		KIRAN SAGAR	
212	IV		MANSOOR ELLAHI	