V. Semester B.C.A. Degree Examination, November/December 2015
(Y2K8 Scheme) (F + R)
Computer Science
BCA – 502 : COMPUTER ARCHITECTURE
(100 – 2013-14 & Onwards) (90 – Prior to 2013-14)

Time : 3 Hours
Max. Marks : 90/100

Instructions: 1) Section A, B, C is common to all. Section D is applicable to the
students of 2011-12 and Onwards.
2) 100 marks for students of 2011-12 and onwards. 90 marks for
Repeater prior to 2011-12.

SECTION – A

I. Answer any ten questions. Each carries two marks. (10x2=20)

1) State and prove Demorgan’s law.

2) Draw the logic diagram of the Boolean function \( F = AB + A'B \) using NAND
gates only.

3) What is Decoder Expansion?

4) What is unidirectional and bidirectional shift register?

5) Convert \((736.4)_8\) to decimal and binary.

6) What is self complementing code and weighted code?

7) What are the two types of control organization?

8) How many bits are needed to specify an address for a memory unit of 4096
words?

9) What is PSW?

10) What is an external interrupt? Give an example.

11) What are peripherals?

12) What is memory management system?
SECTION – B

II. Answer any five questions. Each carries five marks. \(5\times 5 = 25\)

13) Simplify the Boolean function \(F(A, B, C, D) = \sum (0, 1, 2, 5, 8, 9, 10)\) in both sum-of-products and product-of-sums.

14) Design a 4-to-1 multiplexer.

15) Define \(r\) and \((r - 1)\)'s complement. Represent – 14 using Integer representation stored in an 8 bit register.

16) List the micro operations of ADD and ISZ instructions.

17) Explain with a neat block diagram the input-output configuration.

18) Explain register stack with a neat block diagram.

19) What is polling? Explain.

20) Explain Associative memory with a neat block diagram.

SECTION – C

III. Answer any three questions. Each carries fifteen marks. \(3\times 15 = 45\)

21. a) Design a sequential circuit with two JK flip flops A and B and two inputs E and x.

If \(E = 0\) the circuit remains in the same state regardless of the value of \(x\).

When \(E = 1\) and \(x = 1\), the circuit goes through the state transition from 00 to 01 to 10 to 11 back to 00 and repeat.

When \(E = 1\) and \(x = 0\), the circuit goes through the state transition from 00 to 11 to 10 to 01 back to 00 and repeat.

b) Derive the circuit for a 3-bit parity generator using an odd-parity system. \((10+5)\)

22. a) Design a octal to binary encoder.

b) Explain with a neat block diagram a 4-bit bidirectional shift register with parallel load. \((5+10)\)
23) Explain with a neat flowchart the computer operation.  
24) What is Addressing Mode? Explain the different types of Addressing Modes with example.  
25) a) Explain source-initiated data transfer using hand shaking.  
   b) What is virtual memory? Explain address space and memory space in detail.  

SECTION D  

IV. Answer any one questions. Each carries ten marks. (1×10=10)

26) What is binary counter? Explain a 4-bit synchronous counter with a neat block diagram.  

27) a) What are the major characteristics of RISC architecture?  
   b) Explain the block diagram of a computer with I/O processors. (5+5)