I Semester B.C.A. Degree Examination, November/December 2013  
(F+R) (Y2K8 Scheme)  
Computer Science  
BCA 104 : DIGITAL ELECTRONICS  

Time : 3 Hours Max. Marks : 60/70  

Instructions: 1) Answer all Sections.  
2) Section D is applicable to students who have taken admission from 2011-2012 and onwards.  

SECTION – A  

I. Answer any ten questions. Each question carries 1 mark.  
(1×10=10)  
1) State Kirchoff’s voltage law.  
2) What is bilateral network?  
3) Mention the three types of Energy Bands.  
4) Define the term Doping.  
5) Convert (F5A)\textsubscript{16} to octal.  
6) Find the 2’s complement of –34.  
7) Define peak value.  
8) What are combinational circuits?  
9) Write the truth table for EX-OR gate.  
10) What is a flip-flop?  
11) Define Racing condition.  
12) List the different types of shift registers.  

SECTION – B  

II. Answer any five questions. Each question carries 3 marks.  
(3×5=15)  
13) State Ohms Law. Calculate the current flowing across a 3 Ω resistor with a voltage of 12 V power.  
14) Briefly explain about Bohr’s Atomic model.  
15) With a neat diagram explain the operation of P-N junction diode.  
16) Compare TTL with CMOS.  

P.T.O.
17) State and prove De-Morgans theorems.
18) With diagram explain half subtractor.
19) Explain 4 to 1 Mux with diagram.
20) What is delay flip-flop? Explain briefly.

SECTION – C

III. Answer any five questions. Each question carries 7 marks. (7×5=35)

21) State and explain Thevenin’s theorem. 7
22) a) Explain Intrinsic semiconductor. 4
    b) Compare half-wave and full-wave rectifier. 3
23) a) Explain forward bias condition in a diode with characteristic diagram. 4
    b) Write a note on IC families. 3
24) Simplify the following into SOP form using K-Map and realize using gates. 7
    \[ F (A, B, C, D) = \sum m \{0, 1, 3, 8, 12, 13, 14\} + \sum d \{9, 15\} \]
25) Prove NAND and NOR gates as universal gates. 7
26) a) Explain the working of parallel binary adder with diagram. 3
    b) With the diagram explain decimal to BCD encoder. 4
27) a) Explain JK flip-flop with the logic diagram. 4
    b) How do you eliminate racing condition? Explain. 3
28) Briefly explain the different types of shift registers. 7

SECTION – D

IV. Answer any one of the following. Each question carries 10 marks. (10×1=10)

29) a) Explain half-wave rectifier with a neat diagram. 5
    b) Explain parity Generator and parity checker. 5
30) a) Explain the working of adder/subtractor with the diagram. 5
    b) What is RS flip-flop? Explain clocked RS flip-flop. 5